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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,553	06/20/2001	Lars-Peter Heineck	GR 98 P 1379 D	6319

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,553	HEINECK ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,7 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 06/18/2004 forms the basis of this official action. In said Amendment Applicant canceled claims 5 and 6 and amended claims 1 and 7. Applicant previously canceled claim 2. Therefore, claims 1, 3-4 and 7-8 are pending. Comments on Remarks in said Amendment are included below under "Response to Arguments".

Response to Arguments

1. Applicant's arguments filed 06/18/2004 have been fully considered but they are not persuasive.

(a) With regard to the traverse based on the distinction made by Applicant in Remarks between passivation layer and spacer (page 6 of Remarks): the distinction by Applicant between passivation layer and spacer layer on the basis of thickness does not convince, because any oxide layer inherently has a passivating as well as a spacing effect while no particular limit in the thickness is included in the Specification or in the claim language.

(b) With regard to the traverse of reference number 136 as an oxide passivation layer rather than a spacer, said traverse depends on the traverse ad (a). That "not every isolating layer or part of a layer which extends vertically along the gate is a passivation layer" is agreed with but irrelevant, the question merely being whether 136 from its structure and composition has the effect of passivation, with reference to the official action's argument in this regard.

(c) With regard to Applicant's traverse of the interpretation of 138 as a spacer on account of its coverage of a whole surface, when a portion of 138 has the same effect as a sidewall spacer then it could be called immaterial for the spacing function whether or not said portion is, along its longitudinal direction, connected to a region of the same material constitution that, however, because of its different topographical relation to the gate cannot be called a spacer.

(d) With regard to Applicant's argument that "layer 138 is not formed on a passivation layer but on a further silicon oxide spacer 136" again depends on argument ad (a).

Therefore, the examiner regrettably has to make the rejections of the previous official action stand.

However, the amendment to claim 1 and cancellations of claims 5 and 6 together have overcome the objection to claim 1 and the double patenting rejections of claims 5 and 6, which are herewith withdrawn.

Claim Rejections - 35 USC § 102

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. ***Claims 1 and 3*** are rejected under 35 U.S.C. 102(e) as being anticipated by Ahmad (6,037,639). Ahmad teaches (cf. Figure 5 and title, abstract, col. 1, l. 5-10, col. 3, l. 11 – col. 5, l. 50):

a semiconductor substrate 101 (col. 3, l. 19-23) having a substrate surface (upper main surface) (cf. Figure 5), a first conductive region and a second conductive region, namely: source and drain regions 117 (col. 3, l. 37-48);

a gate oxide 108/124 (col. 3, l. 31-37 and col. 4, l. 16-32) disposed on said substrate surface;

a gate 112 (col. 4, l. 16-21) disposed on said gate oxide over an area between said first conductive region and said second conductive region and having side walls adjacent respective ones of said conductive regions (cf. Figure 5);

a silicon oxide passivation layer 136 (col. 5, l. 13-21) disposed on said sidewalls of said gate; and

an insulating silicon nitride spacer 138 (col. 5, l. 44-50) disposed on said silicon oxide passivation layer, said spacer inherently acting as an oxidation barrier by virtue of its material constitution and location (the limitation "said spacer acting as..." constitutes functional language and does not further limit the MOS transistor as device);

said gate oxide insulating said gate from said semiconductor substrate (because said gate oxide is interposed between said gate and said substrate; cf. Figure 5) and having a thickened area 124 (col. 4, l. 16-32) in a region below at least one (in fact both) of said side walls adjacent said conductive regions (cf. Figure 5).

In conclusion, Ahmad anticipates claim 1.

On claim 3: said gate by Ahmad includes a layer selected from the group consisting of a tungsten silicide layer and a polysilicon layer, namely: a polysilicon layer 112 (col. 3, l. 31-37).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claim 4*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad (6,037,639) in view of Sun et al (5,612,249). As detailed above, Ahmad anticipates claim 1. Furthermore, Ahmad does teach not only that said gate includes a polysilicon layer 112 (col. 3, l. 31-37) but also a refractory metal silicide layer 114 (col. 3, l. 31-37). Ahmad does not necessarily teach that said refractory metal silicide layer is a tungsten silicide layer. However, (a) tungsten is a refractory metal, i.e., a metal with a high melting point; while, moreover, (b) it would have been obvious to select tungsten as the refractory metal for the refractory metal silicide layer by Ahmad in view of Sun et al, who teach, in a patent on a method of forming field isolation near a poly gate (cf. abstract), hence closely related art, the selection of tungsten (col. 8, l. 13-17) for its relatively low electrical resistivity as the refractory metal in the refractory metal silicide gate layer on top of the polysilicon gate layer 18. *Motivation* to select tungsten as the refractory metal stems from the enhanced conductivity of the gate line (cf. col. 8, l. 13-17), thus reducing ohmic losses and response time.

4. ***Claim 7*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al and Sun et al as applied to claim 4, and further in view of Krautschneider ((5,854,500). As detailed above, claim 4 is unpatentable over Ahmad in view of Sun et al. Ahmad nor Sun et al necessarily teach the further limitation of claim 7. However, it would have been obvious to include said further limitation in view of Krautschneider: as shown by Krautschneider (front figure), lateral MOS transistors with attributes as taught by Ahmad, particularly with gate oxide 110 (see in Krautschneider column 5, lines 17-26 and column 6, lines 26-27) and nitride side spacers 114 (cf. column 6, lines 45-49), and with a gate of polysilicon (cf. column 5, lines 19-20), for instance, have long been applied as selection transistors to DRAM memory cells (cf. abstract, first sentence), thus constituting an obvious use of the invention by Ahmad. It has to be kept in mind that *motivation* to combine the references also derives from the stated field of application to random access memory devices made by Ahmad (see Ahmad, col. 1, l. 5-10).

5. ***Claim 8*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al (6,037,639 B1) in view of Krautschneider ((5,854,500). As detailed above, Ahmad anticipates claim 1. Ahmad does not necessarily teach the further limitation of claim 8. However, it would have been obvious to include said further limitation in view of Krautschneider: as shown by Krautschneider (front figure), lateral MOS transistors with attributes as taught by Ahmad, particularly with gate oxide 110 (see in Krautschneider column 5, lines 17-26 and column 6, lines 26-27) and nitride side spacers 114 (cf. column 6, lines 45-49), and with a gate of polysilicon (cf. column 5, lines 19-20), for

instance, have long been applied as selection transistors to DRAM memory cells (cf. abstract, first sentence), thus constituting an obvious use of the invention by Ahmad. It has to be kept in mind that *motivation* to combine the references also derives from the stated field of application to random access memory devices made by Ahmad (see Ahmad, col. 1, l. 5-10).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
September 13, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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